**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-22. (canceled)

23. (currently amended) A method for fabricating a power semiconductor device, comprising:

forming a shallow trench on a substrate having a first surface and a second surface, the shallow trench having a first depth and a width, the width of the shallow trench being greater than the first depth of the shallow trench;

forming a doped region provided proximate the first surface of the substrate and having a second depth;

forming a source region provided within the doped region and proximate the first surface; and

forming a gate structure provided adjacent the source region, the gate structure including a first portion provided within the shallow trench and a second portion provide outside of the trench,

wherein the first portion includes a lateral extension and that is parallel to the first and second surface of the substrate,

wherein the lateral extension of the first portion is at least 2.5 times greater than the first depth of the shallow trench,

~~The method of claim 22,~~ wherein forming the shallow trench includes:

etching the substrate to form an intermediate trench having a third depth that is less than the first depth;

forming a first oxide layer within the intermediate layer; and

removing the oxide layer formed within the intermediate trench, wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth.

24. (original) The method of claim 23, wherein an isolation trench is formed in another location on the substrate during the etching step, wherein a second oxide layer is formed within the isolation structure at the same time the first oxide layer is formed within the intermediate trench, the first oxide layer being further processed to be an isolation structure.

25-27 (canceled).

28. (currently amended) A method for fabricating a power semiconductor device, comprising:

forming a shallow trench on a substrate having a first surface and a second surface, the shallow trench having a first depth and a width, the width of the shallow trench being greater than the first depth of the shallow trench;

forming a doped region provided proximate the first surface of the substrate and having a second depth;

forming a source region provided within the first doped region and proximate the first surface; and

forming a gate structure provided adjacent the source region, the gate structure including a first portion provided within the shallow trench and a second portion provide outside of the trench,

wherein forming the shallow trench includes:

etching the substrate to form an intermediate trench having a third depth that is less than the first depth;

forming a first oxide layer within the intermediate layer; and

removing the oxide layer formed within the intermediate trench, wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth.[[.]]

29. (previously presented) The method of claim 28, wherein an isolation trench is formed in another location on the substrate during the etching step, wherein a second oxide layer is formed within the isolation structure at the same time the first oxide layer is formed within the intermediate trench, the first oxide layer being further processed to be an isolation structure.

30. (currently amended) A power semiconductor device, comprising:

a substrate having an upper surface and a lower surface, the substrate having a trench;

first and second doped regions provided proximate the upper surface of the substrate;

a first source region provided within the first doped region;

a second source region provided within the second doped region; and

a gate provided between the first and second source regions, the gate including a first portion extending laterally within the trench, wherein a depth of the trench is no more than a depth of the first doped region,

wherein the gate has a lateral extension and a vertical extension, the lateral extension being substantially greater than the vertical extension to reduce the curvature of equi-potential lines that are defined below the gate and the first and second dope regions, ~~The power device of claim 1,~~

wherein the gate is formed by etching the substrate to form an intermediate trench having a third depth that is less than the depth of the trench[[;]], forming a first oxide layer within the intermediate layer[[;]], and removing the oxide layer formed within the intermediate trench,

wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth.